Electrical Characteristics at T_j=25℃ (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250 A	120	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250 A	1.4	2.0	2.4	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=120V, T_j=25℃	-	-	1	A
		V_{GS}=0V, V_{DS}=120V, T_j=100℃	-	-	100	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=5A	-	20	25	m
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=4.5V, I_D=5A	-	25	31	m
Transconductance	g_{fs}	V_{DS}=5V, I_D=5A	-	20	-	S
Gate Resistance	R_G	V_{GS}=0V, V_{DS} Open, f=1MHz	-	8.5	-	

Dynamic Characteristics

Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=60V, f=1MHz	-	977	-	pF
Output Capacitance	C_{oss}		-	143	-	
Reverse Transfer Capacitance	C_{rss}		-	6.2	-	
Total Gate Charge	Q_g(10V)	V_{DD}=60V, I_D=5A, V_{GS}=10V	-	13.5	-	nC
Total Gate Charge	Q_g(4.5V)		-	7.6	-	
Gate to Source Charge	Q_{gs}		-	2.8	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	2.0	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=60V, I_D=5A, V_{GS}=10V, R_G=10 ,	-	8	-	ns
Rise time	t_r		-	8	-	
Turn off Delay Time	$t_{d(off)}$		-	14	-	
Fall Time	t_f		-	9	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=20A	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	V_R=60V, I_F=5A, dI_F/dt=500A/ s	-	25	-	ns
Reverse Recovery Charge	Q_{rr}		-	91	-	nC

Fig 1. Typical Output Characteristics

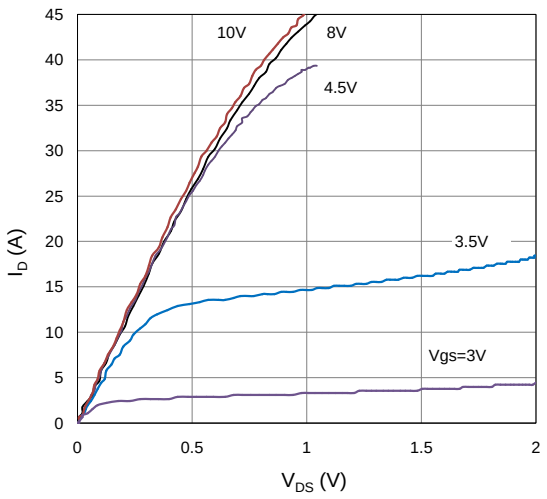


Figure 2. On-Resistance vs. Gate-Source Voltage

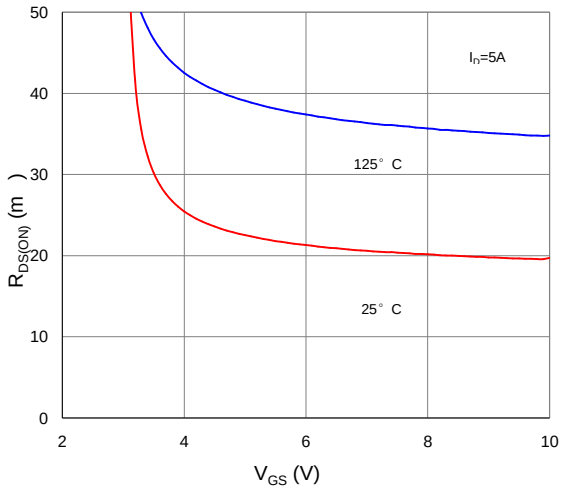


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

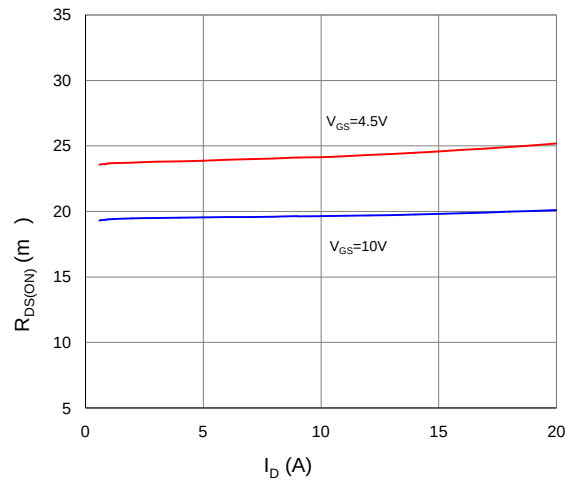


Figure 4. Normalized On-Resistance vs. Junction Temperature

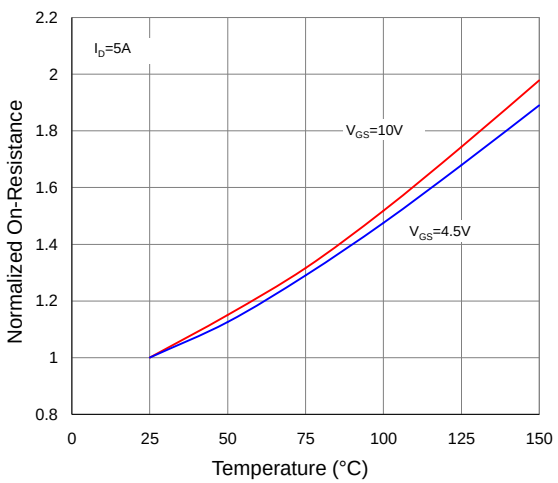


Figure 5. Typical Transfer Characteristics

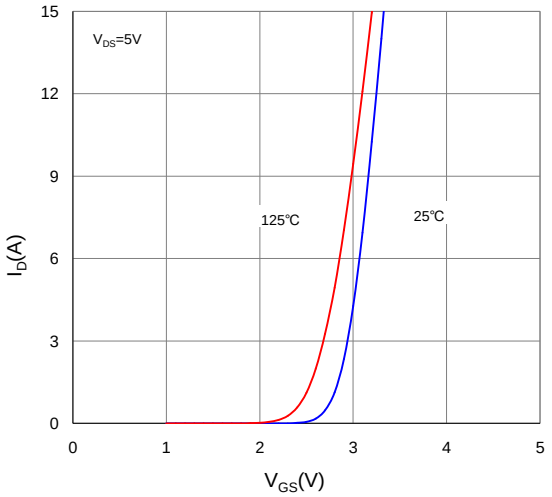


Figure 6. Typical Source-Drain Diode Forward Voltage

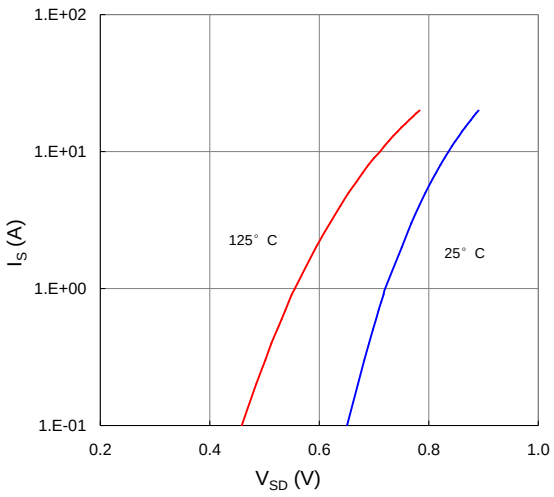


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

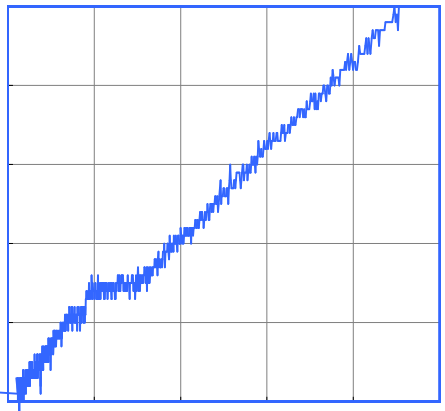


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

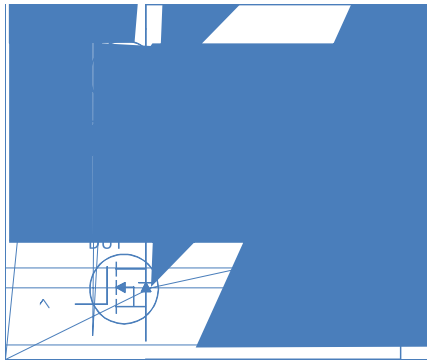
Figure 9. Maximum Safe Operating Area

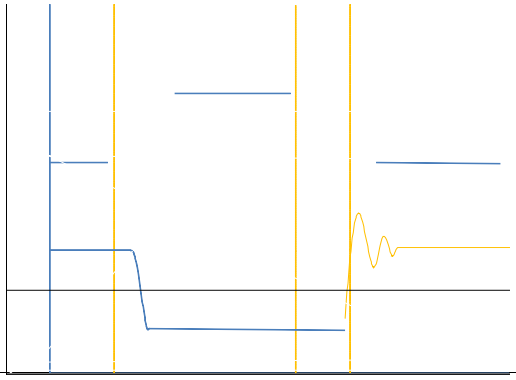
Figure 10. Maximun Drain Current vs. Case Temperature

A

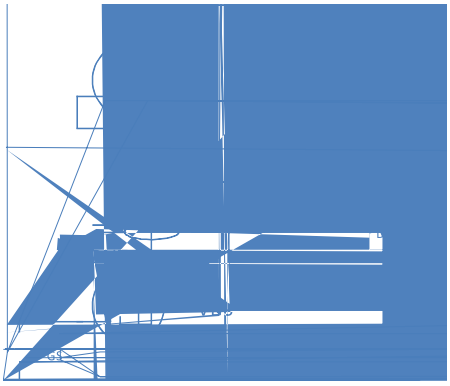
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

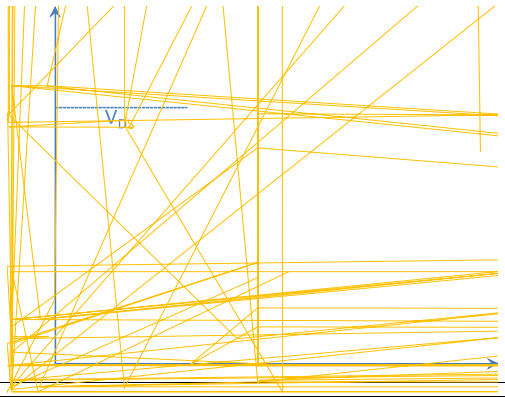
Inductive switching Test



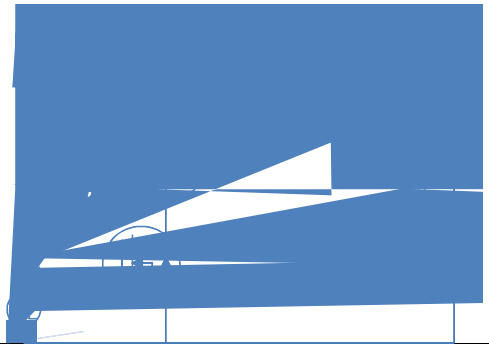


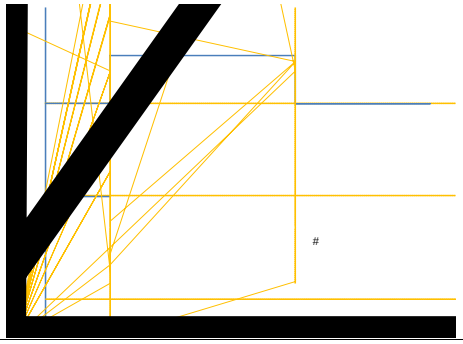
Gate Charge Test



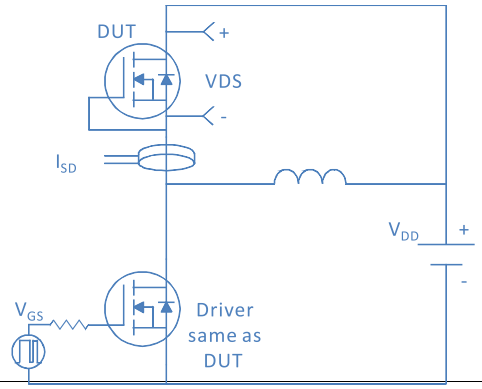


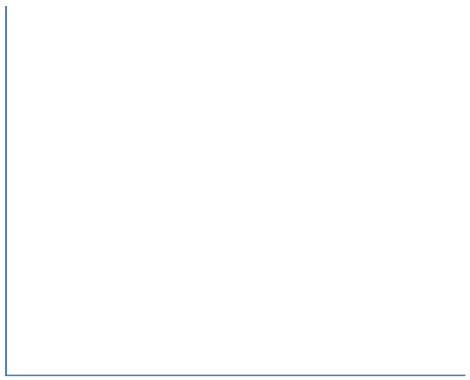
Uclamped Inductive Switching (UIS) Test





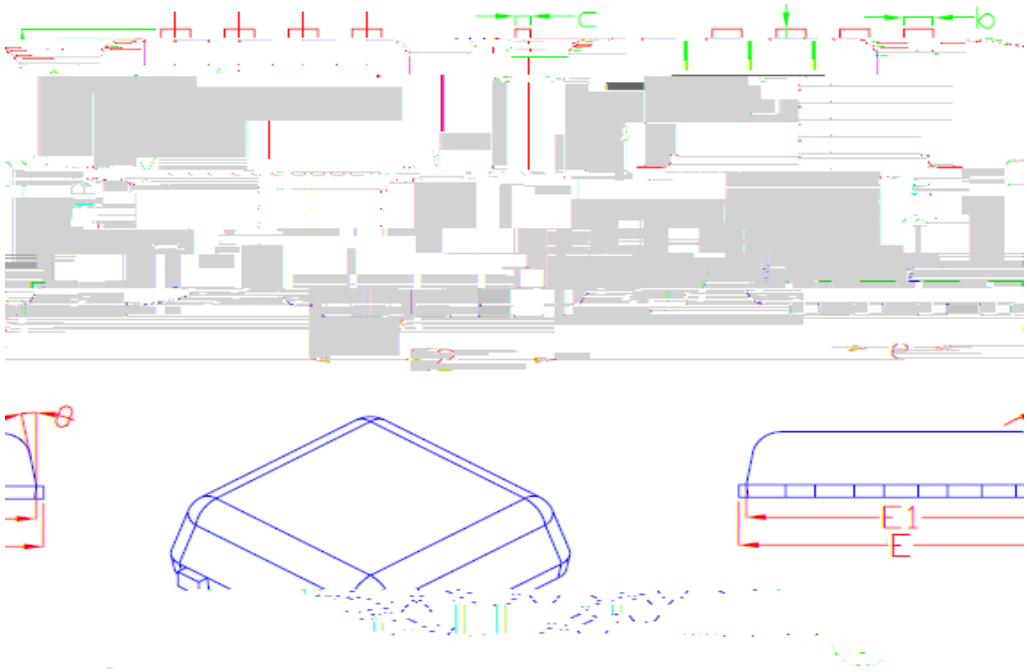
Diode Recovery Test





Package Outline

DFN3.3*3.3_P, 8 leads



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	---	0.13	---
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	---	0.13	---
θ	---	10°	12°
M	*	*	0.15
* Not specified			